

REMARKS

I. Status Of The Claims

Claims 2-11 and 13-58 are pending in this Application.

Claims 4, 5, 15-17, and 23-58 have been withdrawn from consideration.

Claims 2, 3, 6-11, 13, 14, 18-20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirt (U.S. Patent No. 5,883,830) in view of Iwasaki (U.S. Patent No. 5,497,215).

Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirt in view of Iwasaki and Akashi (U.S. Patent No. 5,615,399).

With this response claims 2, 3, 8, 11, 13, 14, 19, and 20 are amended, and claims 6 and 10 are canceled without prejudice or disclaimer. No new matter has been added.

Claims 2 and 14 are independent.

II. Rejections Under 35 U.S.C. 103(a)

The Office Action rejects independent claims 2 and 14 under 35 U.S.C. 103(a) as being unpatentable over Hirt in view of Iwasaki. However, the Applicant respectfully submits that the references, taken individually or in combination, fail to disclose, teach, or suggest all aspects of those claims, at least as amended herewith.

With reference to the Appeal Brief, the Applicant notes that the cited reference Hirt fails, for instance, to disclose, teach, or suggest controlling an accumulation time.

Column 5 lines 58-63 of Hirt, for example, merely discuss a technique where variation of every pixel is canceled by adjusting levels of signals of an image sensor pixel-by-pixel using a common output amplifier. Column 6 lines 46-58 of Hirt, for example, merely

discuss a technique where variation of every pixel is canceled by directly supplying a control signal to a gate of an output transistor of each pixel. Thus, Hirt merely discusses executing a level adjustment by changing a bias of a transistor.

Accordingly, Hirt fails, for instance, to disclose, teach, or suggest a structure that changes an accumulation time for each pixel and a plurality of storage elements.

Turning to Iwasaki, the Applicant notes that Iwasaki merely discusses a structure that controls regions 10a and 10b by using different accumulation time control circuits. Iwasaki fails, for instance, to disclose, teach, or suggest a plurality of storage elements, and fails, for instance, to disclose, teach, or suggest that a storage element is arranged for every photoelectric conversion element. Iwasaki merely discusses a conventional technique described in the background of the invention in the specification of the present application.

As discussed above, the cited references taken individually or in combination, fail, for instance, to disclose, teach, or suggest the feature of the present invention that a storage element is arranged for each photoelectric conversion element and an accumulation time for each photoelectric conversion element is controlled on the basis of information stored in the storage element.

Accordingly, the cited references, taken individually or in combination, fail, for example, to disclose, teach, or suggest:

“... a plurality of storage elements arranged on the same semiconductor substrate, each storing predetermined accumulation period control information employable in controlling a corresponding one of said photoelectric conversion elements, wherein each of said plurality of storage elements includes rewritable memory of which accumulation period control information employable in controlling an accumulation period of said photoelectric conversion element is rewritable by a predetermined program stored in a program memory ...”

as set forth in claim 2 as amended herewith. As another example, the cited references, taken individually or in combination, fail to disclose, teach, or suggest:

“... a controller, wherein said controller controls charge accumulation period of said photoelectric converter on the basis of the accumulation period control information stored in said storage elements”

as set forth in claim 2 as amended herewith.

In view of at least the foregoing, the Applicant respectfully submits that claim 2 at least as amended herewith, as well as those claims that depend therefrom, are in condition for allowance. Moreover, claim 14 at least as amended herewith, as well as those claims that depend therefrom, are thought to be in condition for allowance for at least the same reasons.

III. Dependent Claim Rejections

The Applicant does not believe it is necessary at this time to further address the rejections of the dependent claims as the Applicant believes that the foregoing places the independent claims in condition for allowance. The Applicant, however, reserves the right to further address those rejections in the future should such a response be deemed necessary and appropriate.

(Continued on next page)

CONCLUSION

The Applicant respectfully submits that this Application is in condition for allowance for which action is earnestly solicited.

If a telephone conference would facilitate prosecution of this Application in any way, the Examiner is invited to contact the undersigned at the number provided.

AUTHORIZATION

The Commissioner is hereby authorized to charge any fees which may be required for this amendment, or credit any overpayment to Deposit Account No. 13-4500, Order No. 1232-4478. **A DUPLICATE OF THIS DOCUMENT IS ATTACHED.**

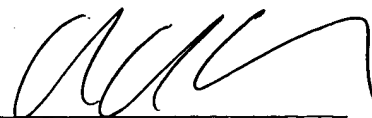
Furthermore, in the event that an extension of time is required, the Commissioner is requested to grant a petition for that extension of time which is required to make this response timely and is hereby authorized to charge any fee for such an extension of time or credit any overpayment for an extension of time to the above-noted Deposit Account and Order No.

Respectfully submitted,

MORGAN & FINNEGAN, L.L.P.

Dated: April 24, 2006

By:



Angus R. Gill
Registration No. 51,133

Mailing Address:
MORGAN & FINNEGAN, L.L.P.
3 World Financial Center
New York, New York 10281-2101
(212) 415-8700
(212) 415-8701 (Fax)